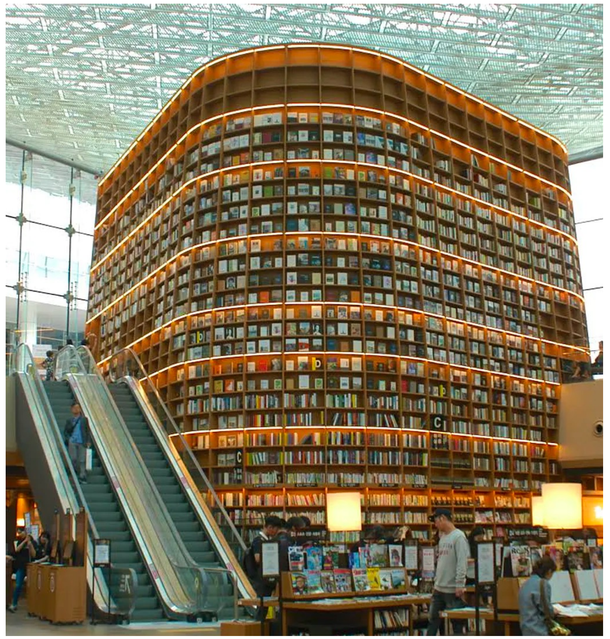
Deploying IC Manage's Highly Integrated IP Catalog at NXP Semiconductors

CadenceLIVE Europe October 2023

What is an IP Catalog?



An organized repository of IP design data that can be used to manage and track usage of IP across multiple SoC projects

IP Should include

- Soft, hard, verification IP
- Memory Compilers
- Foundry IP
- 3rd Party IP
- Firmware/drivers

NXP Background

Long history of delivering diverse products to multiple markets

- NXP, Freescale, Philips, Motorola

Access to many diverse silicon technologies

Numerous IT and design system integrations

Internal systems for capturing and managing IP design data

- Product Lifecycle Management (PLM)
- Tape out management

NXP Problem Statement

PLM, data management and tapeout management systems enable design flows from IP capture to production

Tens of thousands of parts in PLM, not all reusable

A formalized method to identify and flush out metadata for reusable IP was desired

Faster access to key reusable IP data for IP decision makers was desired

NXP Desired Outcome

Streamline steps for IP producers to publish analog and digital IP available for reuse across all product teams

To enable IP consumers with a robust search capability so that finding IP was as easy as using any modern online electronic component web site

Key Challenges

Moving from legacy PLM applications and flows to a modern Web application focused on IP decision makers

Implementing customized search functions with detailed filtering by IP classification, technology node and design parameters

Importing and frequent updates of IP Catalog data from existing NXP data repositories

Provide engineers with the ability to find IP components and assess their compatibility to reuse in new projects

Key Challenges (cont'd)

New Web UI to capture key IP properties (metadata) to enable a consistent and reliable search platform

Agreement on uniform requirements for IP publishing to streamline IP publishing for search and reuse

Intuitive workflow to progress the IP through multiple stages - from initial capture to published for reuse and tracing effectiveness of reuse

Development of a common data model for a diverse set of teams

Integration with existing platforms in a low-cost, reliable way

Achieving Consensus

Clear goals on what we wanted to achieve with the IP Catalog

Workshop with IP providers and decision makers

Robust initial spec and use cases

Multiple rounds of acceptance testing

High focus on application performance and UX

Commitment to data load automation

Getting from Spec to Production

Fast IC Manage updates to development and test environments

NXP ability to update IP Catalog schema directly

Early access to application prototype & rapid iteration on use cases & implementation

2 phases of User Acceptance testing

Unique Capabilities from IC Manage

Graph database improves development productivity AND application performance

User maintainable IP Metadata Schema

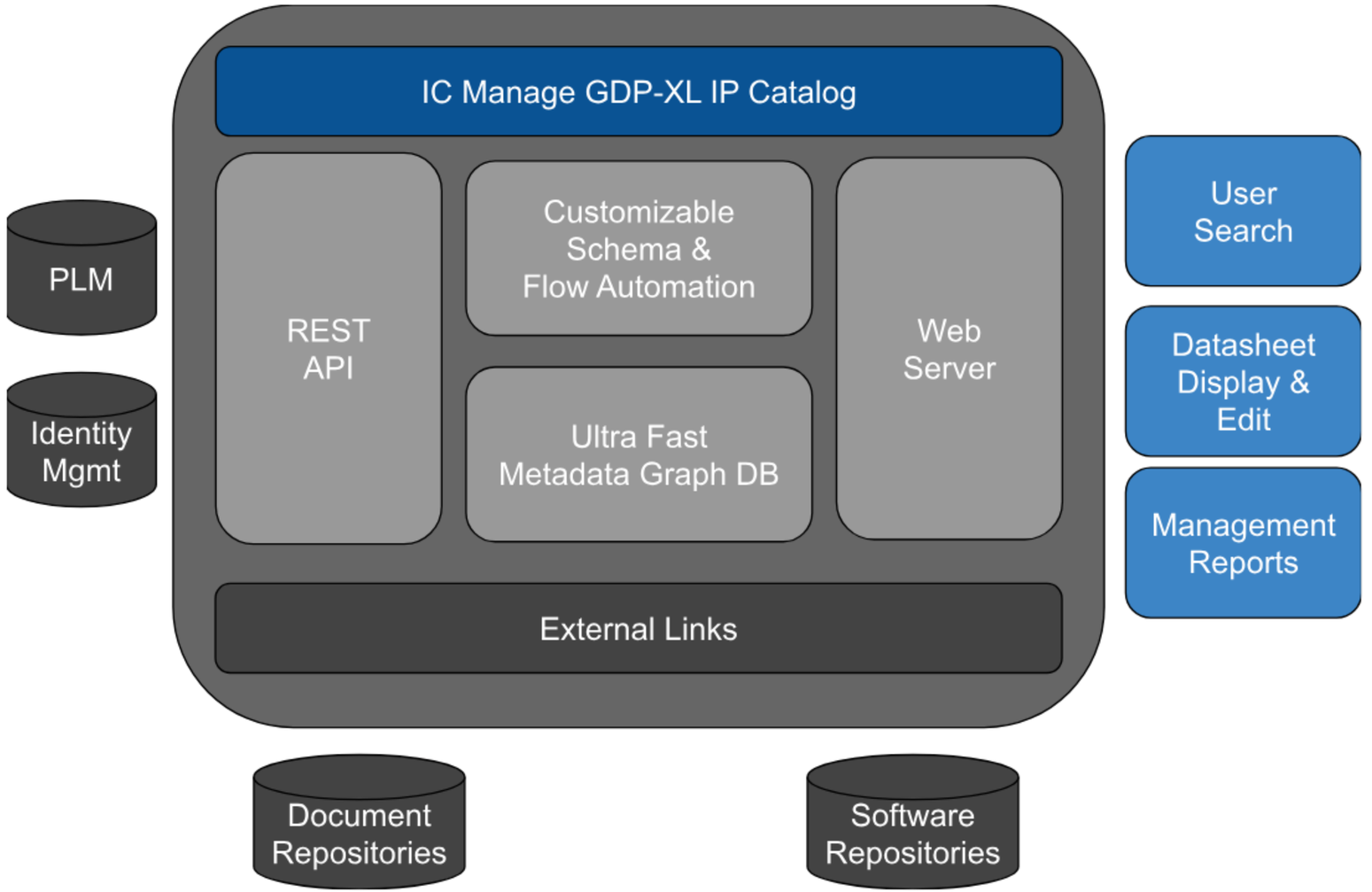
- Schema upload via JSON file
- Schema verification before commit
- No Code UI updates

Unique Capabilities from IC Manage

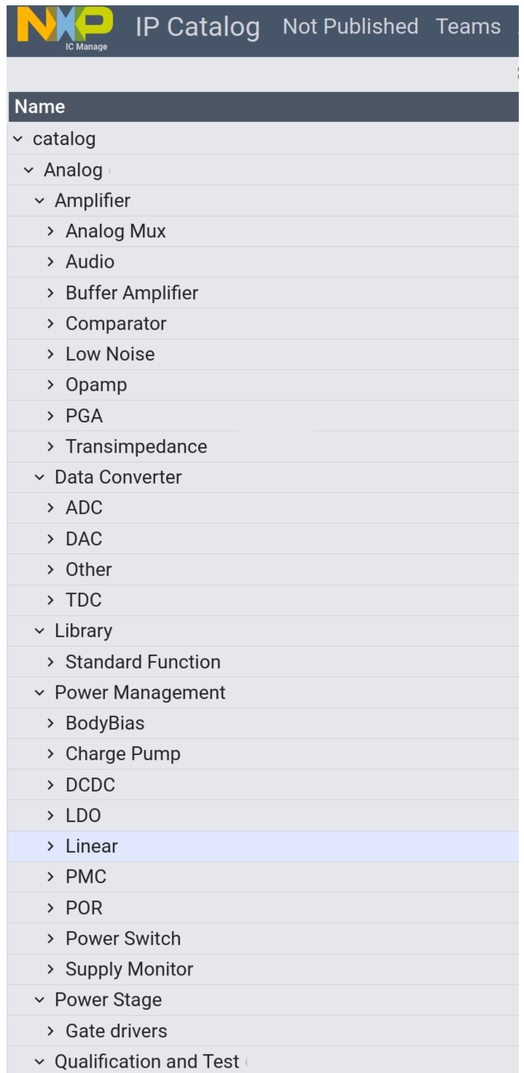
Robust automation framework & Web API for integrating updates from external systems

Strong semiconductor domain and data management development and support experience

IP Catalog Architecture



IP Classification Navigation



Datasheet Rendering from JSON Schema

Summary *

Functional Classification
/catalog/Analog/TimingDevice/PLL

IP Primary Function
Clocking block designed to meet customer X requirements.

Owning Team
Analog IP

Keywords
- Pre-Publish Test

Reuse Maturity Summary
Intended for Wide Reuse

Reuse Summary Statement
Meant for reuse

Support Level
Questions Only

Feature List
- High speed clock
- Low voltage

Dependencies
- digital timer

Parameterization / Configurability
fully configurable

IP Cluster / IP Complex Info
pll cluster

Silicon Maturity Summary
Mature

Available Standard Views
- Cadence Virtuoso OpenAccess
- GDSII
- Power Analysis

Available Tool-Specific Views
- ams

Contacts
- (scott)

Tools and Standards Compatibility *

Implementation Tool Flow
- ams

SoC Assembly
- Hard Macro

NXP Design Environment
- test

Industry
- IBIS

Emulation
- High speed

Verification/Simulation Testbench
- Stingray

External Interconnect Interfaces
- CAN

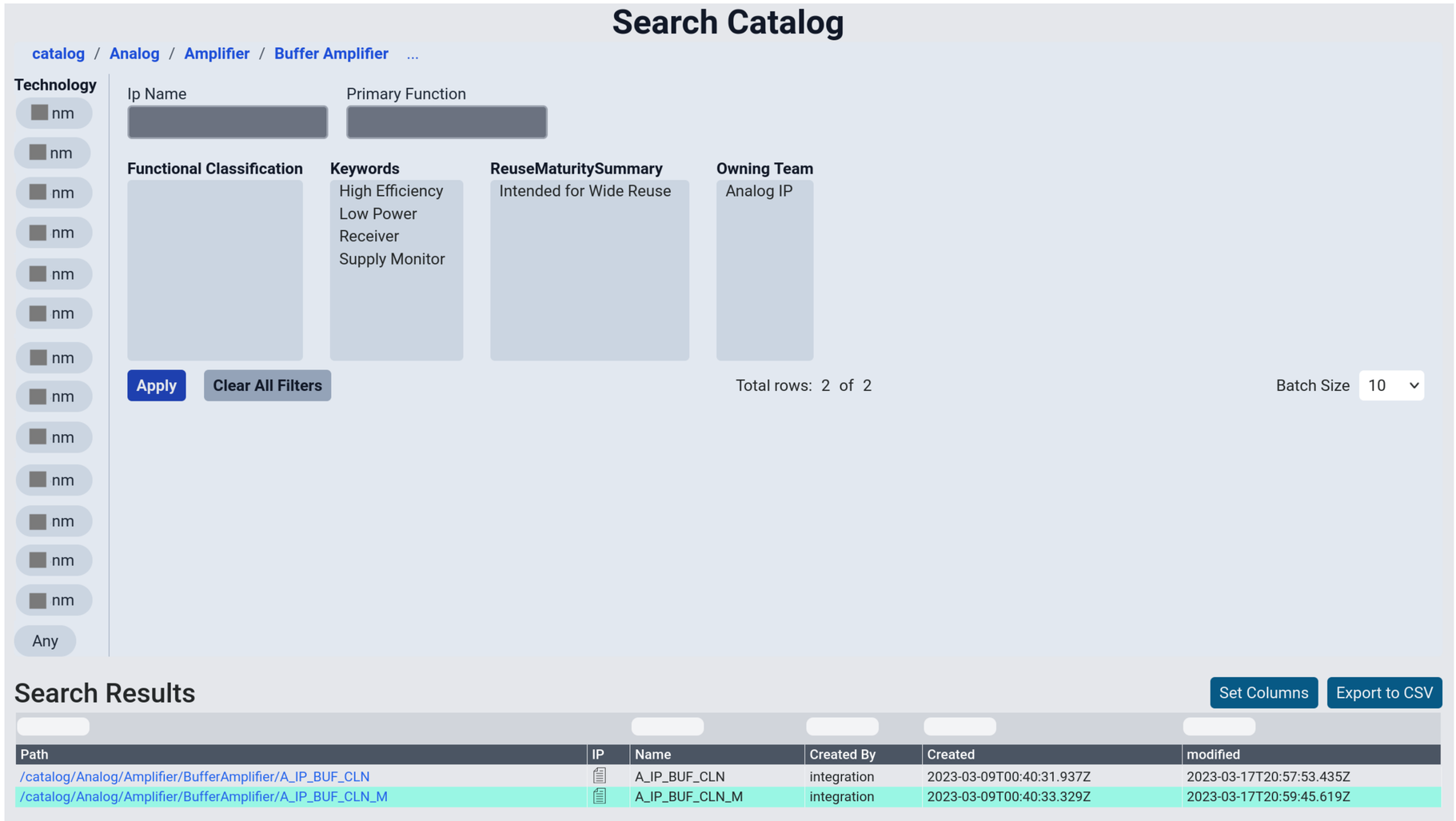
SOC Interconnect Bus Interfaces
- DCR

AEC-Q100 Grade
0 (-40C to 150C)

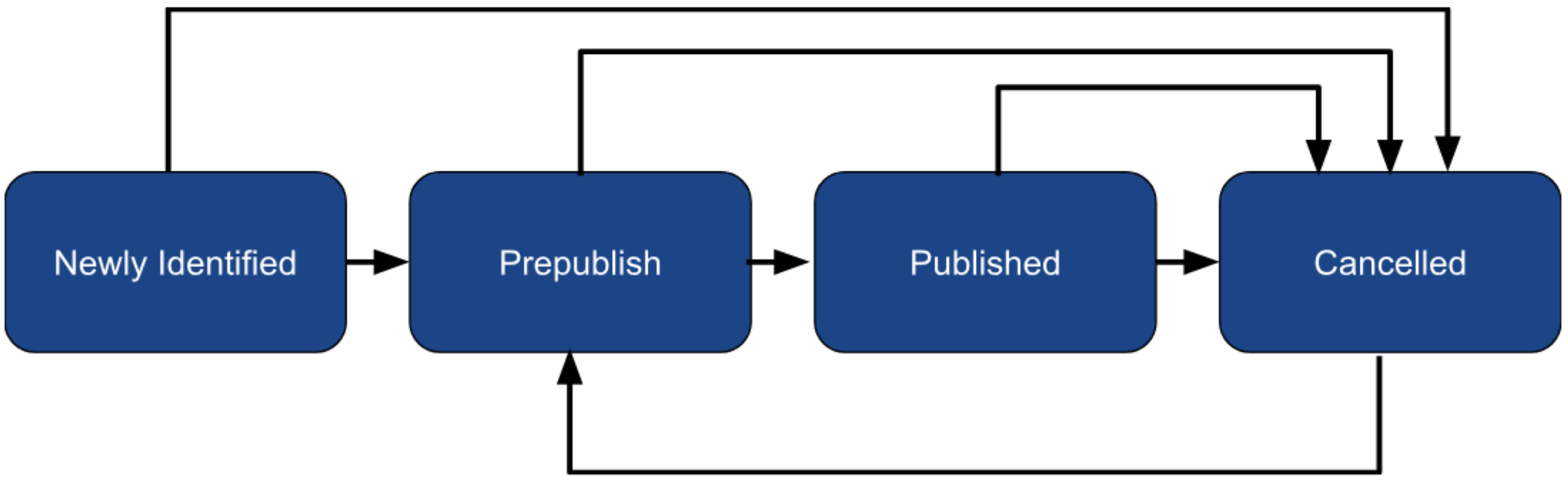
Automotive
ASIL-B

Security Certifications
EL100

Search Page Rendering from JSON Schema



IP Lifecycle State Diagram



Datasheet – Connections to External Data

Documentation *

IP Brief	IP Brief Link	Data Sheet	Data Sheet Link
Yes	http://test.com/ipbrief	Yes	http://test.com/ipdatasheet
User Manual / Integration Guide	**User Manual / Integration Guide Link**	**Requirements Specification**	**Requirements Specification Link**
Yes	http://test.com/ipintergration	Yes	http://test.com/ipspec
Architecture Documentation	**Architecture Documentation Link**	**Verification Specification**	**Verification Specification Link**
Yes	http://test.com/iparch	Yes	http://test.com/ipverifspec
Reference Manual / Block Guide	**Reference Manual / Block Guide Link**	**Application Notes**	**Application Notes Link**
Yes	http://test.com/ipblockguide	Yes	http://test.com/ipappnotes
Errata Documentation	**Errata Documentation Link**	**Release Notes**	**Release Notes Link**
Yes	http://test.com/iperrata	Yes	http://test.com/ipreleasenote
Release Checklist	**Release Checklist Link**	**IP Design FMEA**	**IP Design FMEA Link**
Yes	http://test.com/ipchecklist	Yes	http://test.com/ipfmea

Verification / Validation *

View Generation QA Reports	Verification Reports	Validation Reports	QMS Checklist Report
http://test.com/qareports	http://test.com/verifreports	http://test.com/validationreports	http://test.com/qmschecklistreports

NXP Results from IC Manage IP Catalog

IP Catalog is a rallying point for the diverse IP development and Product teams

IP Catalog is centerpiece of a new company-wide governance process to identify, promote and maintain reusable IP information

Teams discovered interesting IP from other areas of the company during the development and testing period

IP developers and decision-makers appreciate high performance and modern user interface

NXP Results from IC Manage IP Catalog

Automated linkage to NXP's IP & SOC design configuration management platform ensures consistency in basic IP information and a constant feed of new potential candidates for the IP Catalog

Flexibility provided by the database design enables the governance team to manage data model updates without complex IT releases, and the powerful API enables high levels of automation of data import and maintenance

IP reuse is an inherently difficult topic due to competing demands on IP developers' time, and the IP Catalog is now a key part of NXP's journey to fully leveraging its investment in IP development

Summary – Effective IP Catalogs Require

Flexible IP data and metadata models

Tight, automated integration to design and verification flows

Consistency to enable IP to be found and reused

Secure, high performance infrastructure to minimize overhead, prevent IP theft