Implementing a Semiconductor IP Catalog to Enhance IP Accessibility and Reuse to Reduce Product Development Costs and Improve Product Quality

By

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BACKGROUND

NXP has a long history of delivering products to multiple markets with access to many diverse silicon technologies. Several years of M&A has provided NXP with a diverse set of analog, mixed-signal and digital IP development teams and many years of IP development to leverage. As part of this evolution, the combined company also dealt with numerous IT and design system integrations and developed multiple internal solutions for capturing and managing large amounts of IP and SoC design data, Product Lifecycle Management (PLM) and chip tape out management.

PROBLEM STATEMENT

While NXP had deployed these various systems to coordinate the management of design data and capture analog and digital design IP, the design methodology teams also saw a need to formalize a uniform IP publishing and reuse workflow. The goal was to streamline the steps for IP producers to make analog and digital IP available for reuse across all product teams and to enable IP consumers with a robust search capability so that finding IP was as easy as using any modern online electronic component web site.

KEY CHALLENGES

Several custom applications had been developed over 20+ years at NXP, but an easy to use search function with detailed filtering by IP classification, technology node and design parameters was not available.

To provide engineers with the ability to find IP components and assess their compatibility to reuse in new projects, existing NXP data repositories would need to be extended to capture key IP properties (metadata) and augmented with Web based interfaces to enable a consistent and reliable search platform.

Effective IP discovery requires two methods of search:

- A general purpose web-like search across an entire IP Catalog for any occurrence of a string/value of interest
- A component catalog-like search that allows the user to filter by IP classification (analog, digital, amplifier, etc.) and specific properties like technology node or IP maturity

Uniform requirements for IP publishing needed to be defined so that the user would be guided in completing those requirements so that their IP could be found and reused.

An intuitive workflow was needed to progress the IP through multiple stages - from initial capture to published for reuse and tracing effectiveness of reuse.

KEY REQUIREMENTS

Hierarchical IP classification with Customizable IP properties and IP search for any IP classification plus enforcement of publishing criteria so data integrity is assured.

Detailed access and operational control policies to assign permissions to specific user groups for specific IP Categories or to specific users for individual IPs.

Flexibility so that the data organization can evolve without software updates.

Responsibilities for publishing and support need to be decentralized to remove any IP publishing/usage bottlenecks.

Integration with multiple internal PLM and Identity Management systems to enable continuous data updates 24x7 without administrative intervention.

Reference links to design documents and software containers stored in external document management & version control systems to enable deeper study of IP details.

Web UI with high performance and easy to use interface to work like traditional electronic component online stores.

Up to date listing of SoC tape outs for a given IP.

Regular management reports on IP Reuse status.

SOLUTION EXPLORATION

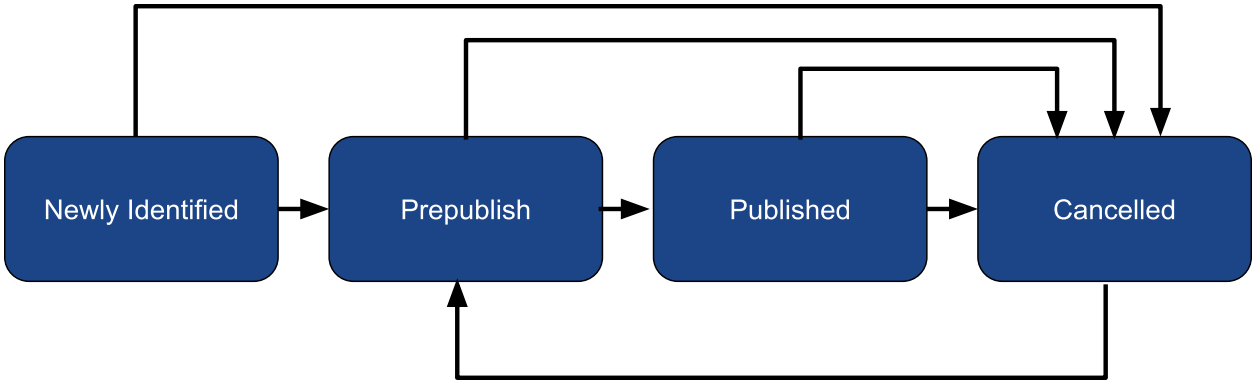
IC Manage has helped the industry's largest semiconductor teams to efficiently solve difficult data and IP management problems. While NXP had legacy data management, tapeout management, and PLM systems in place, the requirement for a usable and searchable IP catalog had not yet been solved. In assessing their options for commercial solutions and internal development, NXP was impressed by IC Manage's Global Design Platform (GDP-XL) that had been architected to enable very flexible workflows, data organization, and the ability to integrate multiple data sources into an easy to use Web-based user interface.

"We engaged with IC Manage because of their exemplary track record and their expertise in design and IP management," said Udi Landen, Vice President of Engineering Design Enablement at NXP, "IP reuse is inherently difficult due to competing demands on IP developers' time, the variety of historic designs, and the quantity of different methodologies involved. With IC Manage we were able to deliver a global IP Catalog as a key part of NXP's strategy and fully leverage the value of our IP."

SOLUTION DEVELOPMENT

After selecting GDP-XL, the IC Manage application team worked with NXP to help define a solution specification and configurable prototype to engage a wide range of design teams representing 1000's of NXP engineering staff, Design Enablement and the CTO office. Rapidly iterating this prototype enabled NXP to finalize its data organization, configure its IP reuse workflow and integrate external data sources to deliver a production system that can be accessed by the entire IC design community. "We were very pleased that the promise of the GDP-XL architecture and the technical team from IC Manage exceeded our expectations in terms of ease of integration, responsiveness and product quality," said Andy Espenscheid Sr. Manager, Hardware Design Enterprise Software, "Our investment in deploying the GDP-XL IP Catalog will yield long term benefits in achieving higher levels of IP Reuse at NXP."

The first detail to resolve was to specify an IP Workflow. This enables the GDP-XL IP Catalog to act as a staging area for new IP to be reviewed, assigned to the appropriate owner and define its properties like IP classification, tool views included and foundry kit requirements to meet the predefined criteria for admission into the IP Catalog.



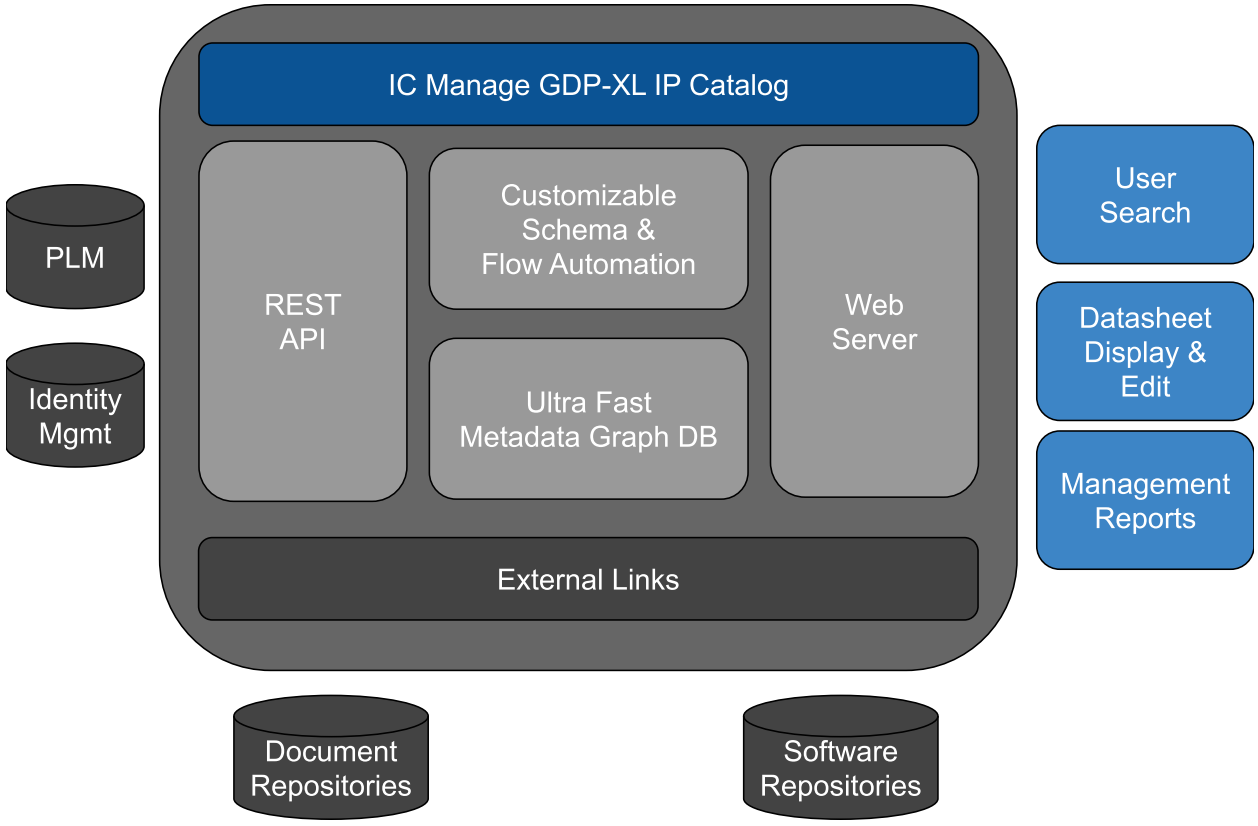
An important part of this IP Workflow is to assign access and modification roles.

- IP Curators have global access privileges, start with the newly identified IP, and then assign it an IP Classification like RF/Amplifier with an owning engineering group plus one or more IP owners so that it can move into the Prepublish state.
- IP Owners then add the necessary IP properties to move it into the Published state so that it is deemed ready for reuse and will be visible in IP search results by the general user community.

It is also possible to cancel an IP as part of the workflow. In this case, the IP is not deleted, but will no longer appear in search results. An IP Curator can later decide to reactivate a canceled IP without having to recreate the IP or its property metadata.

The 2nd key task was to define an IP metadata schema to represent the key properties and metrics so that engineers reviewing IP can find all relevant information on a single page. NXP had a number of existing systems that captured some of this metadata already, but additional fields were required to provide a rich enough set of properties for meaningful, iterable, IP search refinement along with a complete, dynamically rendered datasheet. It was also necessary to define which properties should be static (read only), which would be updated from external data sources or modifiable by authorized staff, and which required integration with corporate identity management systems. Furthermore the schema needed a way to define these requirements as a function of the IP type (S/W, Analog, RF etc). This ensured that engineers reviewing published IP could rely on consistency in the data provided for each similar type of IP.

NXP had existing PLM, issue tracking, tapeout tracking, document and data management systems that captured some of this metadata already, but additional fields were required to provide a rich enough set of properties for meaningful, iterable, IP search refinement along with a complete, dynamically rendered datasheet. It was also necessary to define which properties should be static (read only), which would be updated from external data sources or modifiable by authorized staff, and which required integration with corporate identity management systems.



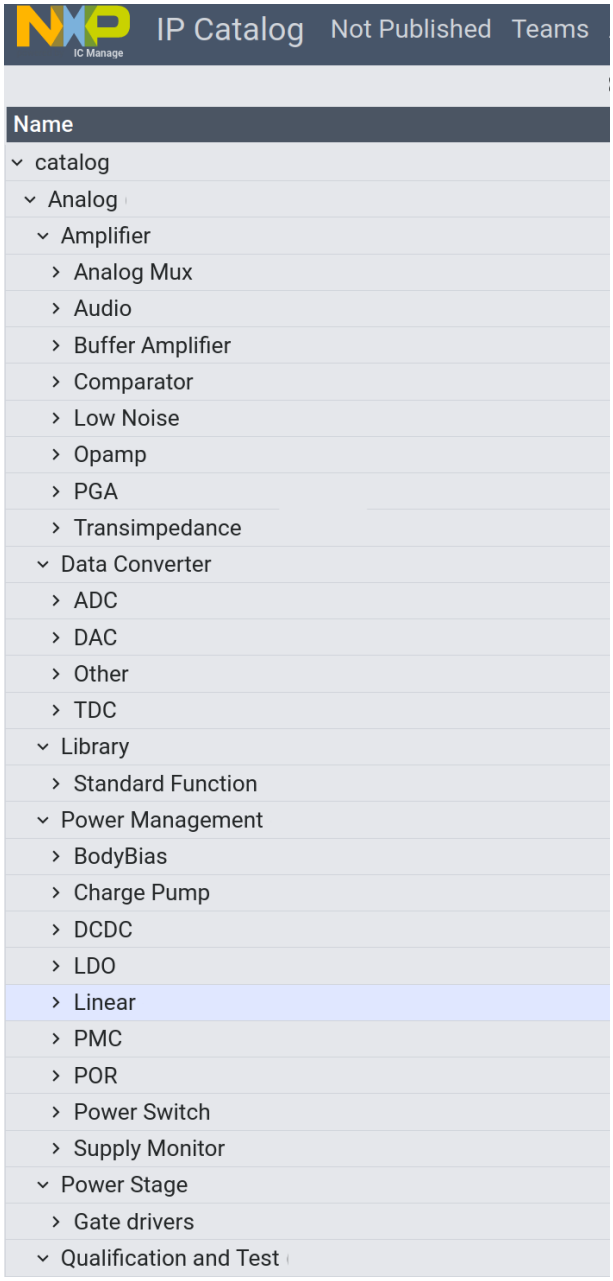
The last stage of development was to integrate the external PLM and data and tapeout management systems. This allowed data changes to propagate automatically into the IP Catalog to ensure that all search results and IP Datasheet summaries represent up to date information. While this data originates from multiple systems, it is presented in a single page for the end user.

This task was very straightforward since GDP-XL has an object oriented API that operates on IP and its properties as direct objects, even for complex data structures with dozens of data fields that can be queried or updated with a single command. It also allows reports to be generated for multiple IPs that meet specific criteria (like all Amplifiers in a classification category) and return a set of specified properties in a single command.

KEY GDP-XL CAPABILITIES

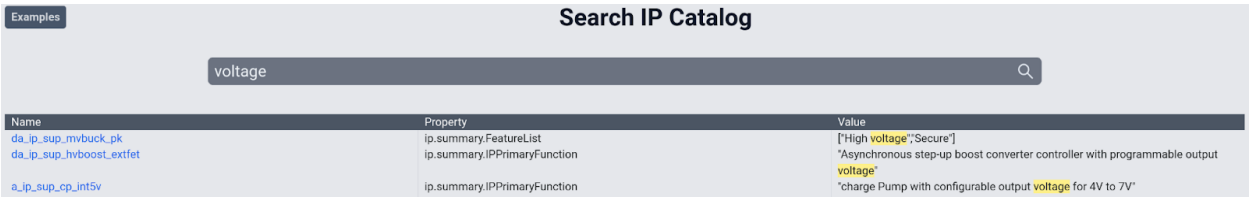
GDP-XL provided many key configurable capabilities that facilitate end user customization without having to create an NXP-only application:

Classification Hierarchy to logically organize IP functionality

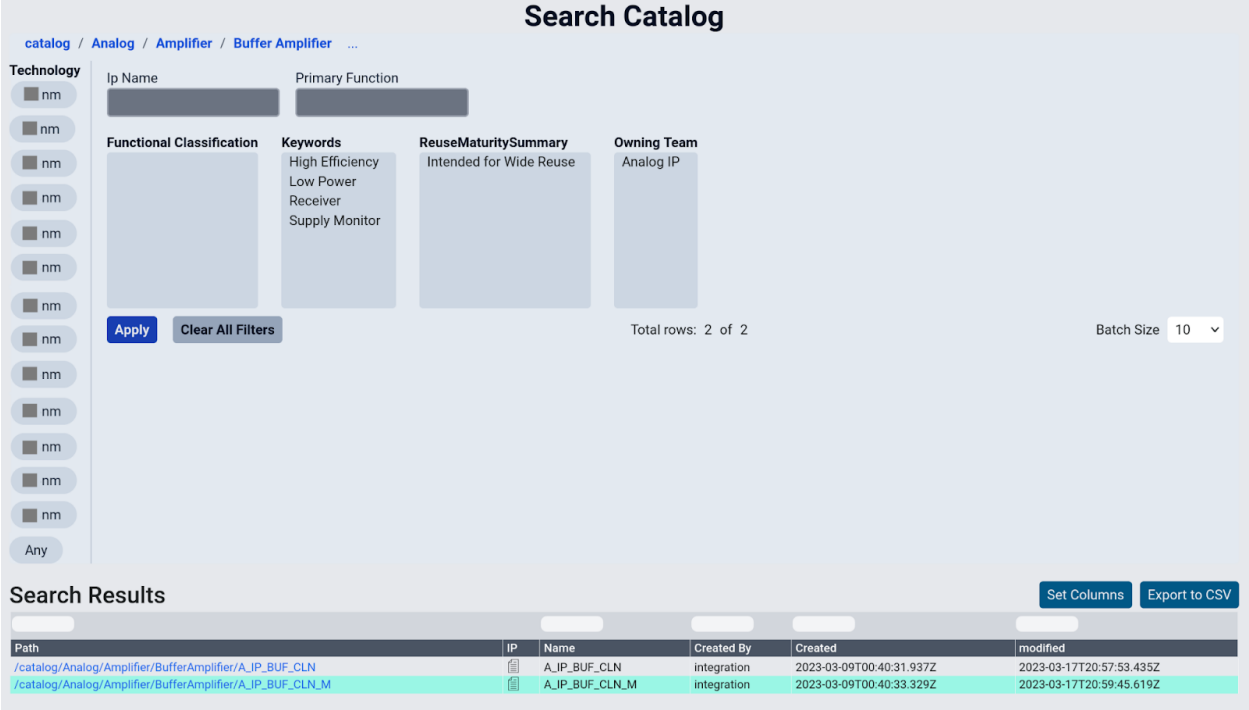


Hierarchical IP Metadata Schema to enable classes of IP properties to be grouped together
Schema driven Web UI layout that dynamically renders customized IP datasheets

Generic search to find any occurrence of a string in any published IP



Schema driven Advanced Search pages that can be uniquely configured for each IP classification and allow users to apply filters to narrow down their IP choices



Links to external data sources to easily navigate to design document and software repositories REST API integration of existing PLM systems to enable a full view of all relevant IP related data, even if it is captured and updated in other systems

Documentation *

IP Brief	IP Brief Link	Data Sheet	Data Sheet Link
Yes	http://test.com/ipbrief	Yes	http://test.com/ipdatasheet
User Manual / Integration Guide	**User Manual / Integration Guide Link**	**Requirements Specification**	**Requirements Specification Link**
Yes	http://test.com/ipintergration	Yes	http://test.com/ipspec
Architecture Documentation	**Architecture Documentation Link**	**Verification Specification**	**Verification Specification Link**
Yes	http://test.com/iparch	Yes	http://test.com/ipverifspec
Reference Manual / Block Guide	**Reference Manual / Block Guide Link**	**Application Notes**	**Application Notes Link**
Yes	http://test.com/ipblockguide	Yes	http://test.com/ipappnotes
Errata Documentation	**Errata Documentation Link**	**Release Notes**	**Release Notes Link**
Yes	http://test.com/iperrata	Yes	http://test.com/ipreleasenote
Release Checklist	**Release Checklist Link**	**IP Design FMEA**	**IP Design FMEA Link**
Yes	http://test.com/ipchecklist	Yes	http://test.com/ipfmea

Verification / Validation *

View Generation QA Reports	Verification Reports	Validation Reports	QMS Checklist Report
http://test.com/qareports	http://test.com/verifreports	http://test.com/validationreports	http://test.com/qmschecklistreports

PROJECT USAGE REPORTING

Product Tapeout Info *

Entries

SOC Master	SOC Design Name	SOC Technology
bcc_SMOS_HV	bcc	SMOS_HV
24v_SMOS_HV	24v	SMOS_HV
smoke_test	smoke_test	SMOS_HV

REPORT GENERATION

GDP-XL's API and Command Line Interfaces provide very simple syntax options to generate IP reports across the entire repository or any subsection and return one or more of the 100+ IP properties in table form, CSV for spreadsheets or JSON for integration into external processing scripts or enterprise systems.

New Pre Published Cancelled

Name	Status	Owning Team	Functional Classification	Type
A_IP_PLL_FM_F3	pre-publish	Analog IP	/Analog/TimingDevice/PLL	Design IP Master
DA_IP_DDR_LP	pre-publish	Digital IP	/Mixed-Signal/MemoryController/RAM	Design IP Master
D_IP_BTU_SYN	pre-publish	Digital IP	/Digital/Wireless/BT-BLEController	Design IP Master
D_IP_IDA_IRQ_LIMITER	pre-publish	Digital IP	/Digital/CoresandPlatform/ProcessorSupport	Design IP Master
D_IP_SSI_CHASSIS_SYN	pre-publish	Digital IP	/Digital/Communication/SystemLevelInterconnect	Design IP Master
S_IP_IDA_GLOBALCTRL_SYN	pre-publish	Digital IP	/Digital/CoresandPlatform/ProcessorSupport	Design IP Master
S_IP_IDA_MTR_SYN	pre-publish	Digital IP	/Digital/MemoryInterfaceExternal/MTR	Design IP Master
S_SOC_IDA_HSI_ETHERNET_PCI	pre-publish	Digital IP	/Digital/HighSpeedSerial/PCIe	Soc Master
S_SOC_IP_IDA_SLIC	pre-publish	Digital IP	/Digital/Communication/SystemLevelInterconnect	Soc Master

SUMMARY

NXP deployed the IC Manage GDP-XL IP Catalog to its entire IC design community which enabled efficient workflow for 1000's of IP producers and to create, update and publish 1000's of IPs so that project architects and integrators can easily find, compare and leverage reusable IP to minimize product development costs. The customizable, Web based IP search interface is now the main path to quickly find IP and filter search results based on a wide set of IP classification types and properties.
Engineering management benefits from having up to date progress reports on levels of IP Reuse compatibility as well as levels of reuse across multiple products.

Some examples of the types of queries that can be processed:

- Find & Sort IP by security restrictions
- Find IPs by the external IP provider, which tapeouts have used it and any financial obligations
- Search for IP based on compliance standard like (ASIL-D)
- Search by keywords, features, regular expressions, maturity level
- List all IPs owned by a specific group or individual

Some examples of actions that can be taken with search results or on IP datasheets:

- View which design views (schematic, layout, netlist, etc.) are included in an IP
- Customize search page to add additional result columns
- Click on link to architectural specification, Reference Manual
- Navigate to firmware git repository
- Export search results to CSV

RESULTS

NXP has a diverse product portfolio and a correspondingly diverse set of IP teams. The IP Catalog project has served as a rallying point for these teams. The IP Catalog is the centerpiece of a new company-wide governance process to identify, promote and maintain reusable IP information. Even during the development and testing period, teams discovered interesting IP from other areas of the company. The IP developers and decision-makers have appreciated the high performance and modern user interface of the IP Catalog. The automated linkage to NXP's IP & SOC design configuration management platform ensures consistency in basic IP information and a constant feed of new potential candidates for the IP Catalog. The flexibility provided by the IP Catalog database design enables the governance team to manage data model updates without complex IT releases, and the powerful API enables high levels of automation of data import and maintenance. IP reuse is an inherently difficult topic due to competing demands on IP developers' time, and the IP Catalog is now a key part of NXP's journey to fully leveraging its investment in IP development.